Final Project Report

Analog IC design

B05901088 黃士銘

(a) Design Procedure

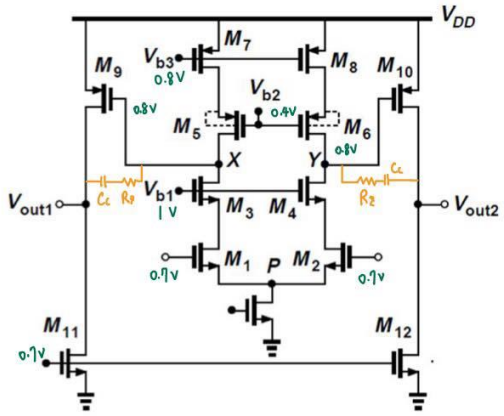


Fig. 1 Op-amp Structure

1. Gain Arrangement

Telescopic Op should produce larger gain than the second stage. Originally, I set **the first stage gain to be 150 and the second stage gain to be 20.**

2. Current Arrangement

The total power should not exceed 2mW, thus the total current should not exceed $\frac{2\text{mW}}{1.5\text{V}} = 1.33mA$. At the first glance, I thought that the 2pF load at Vout would be harder for the second stage to drive.

Therefore, I **arrange 0.5mA for the first stage** and **0.8mA for the second stage.** However, in the final optimization, the current of the second stage can be cut down to 0.5mA as well.

3. First Stage Vov Design

Suppose that the gain of the second stage is 20. The first stage output swing should be at least $\frac{0.75\text{V}}{20} = 0.0375\text{V}$.

Supposed that I reserved 0.1V for deep-triode-current- source MMI, and 0.1V for the output swing, I still have $\frac{1.3\text{V}}{4} = 0.325\text{V}$ reserved for $\text{M}_{1\sim8}$, it is way to big than necessary. Thus I set $\mathbf{Vov} = \mathbf{0.2V}$ **for** $\mathbf{M_{1\sim8}}$ **in the end.**

4. First Stage Aspect Ratio

After the determination of current and Vov of each transistor, I can calculate the aspect ratio of all transistors.

5. Second Stage Vov Design

$\text{V}_{\text{sg9,10}}$ would be determined by $\text{V}_{\text{x,y com}}$. In this case, $\mathbf{V_{sg9,10}}$ **is 0.8V**. With the Implementation of CMFB loop in the second stage(red lines in Fig.1), the $\mathbf{V_{gs11,12}}$ **is at 0.7V.**

6. Second Stage Aspect Ratio

With $\text{V}_{\text{g,s}}$ and current budgets determined, the aspect ratio can also be calculated.

7. Improving Output Resistance

Amid the design, I was frustrated by the gain of first stage. After the examination of output resistance in .lis file, I discovered that the output resistance of NMOS is only a third of PMOS. Therefore, **I tripled the W and L of NMOS**, and the gain boosted a lot.

8. Phase Margin Improvement

Without any capacitor compensation, there was no phase margin left for the circuit.

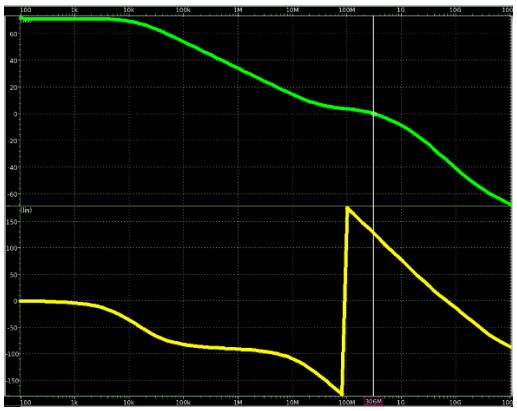


Fig. 2 Gain/PM of original Op-amp

The unity gain frequency should be 34MHz so as to get 60^0 phase margin. Rout of the first stage is $68\text{k}\Omega$ and the gain of the second stage is 23. Therefore, the Miller's compensation Capacitor should be:

$$\text{Cc} = \frac{1}{\text{Rout} \cdot \omega_{3\text{dB}} \cdot \text{Av}_2} = \boldsymbol{10pF}$$

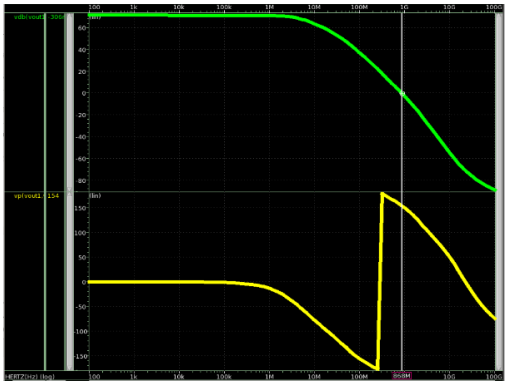


Fig. 3 Gain/PM with Miller's Compensation

Because of another zero introduced by gm9 and Cc, there is still no phase margin left. A Rz is needed to compensate the new zero:

$$\text{Rz}_{\text{thm}} = \frac{1}{\text{gm}_9} \approx 500$$

The Bode' plot then looks like a simple pole system. **Phase margin reachs $\boldsymbol{80^0}$**, which is very stable.

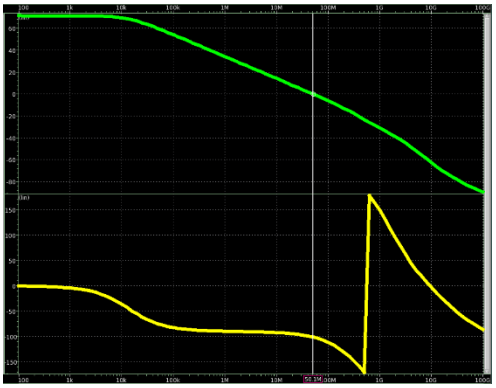


Fig. 4 Gain/PM of Op-amp with Cc and Rz

(a) Common Mode Feed Back

1. First Stage

The First Stage CMFB Loop is shown with Blue line. R1 and R2 would sense the common mode of Vx and Vy, which would become the gate voltage of MMI. The design flow of this circuit is listed below:

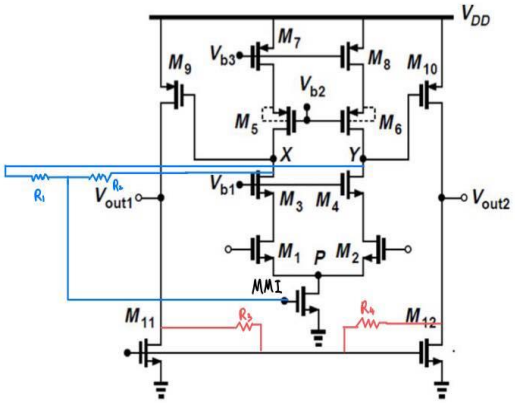


Fig. 5 CMFB Circuit of Op-amp

1. Select big resistance (1Meg) to construct the DC voltage of the whole circuit.
2. Examine .lis file and calculate Rout at Vx. R1 and R2 should only be comparable to Rout, thus they can be reduced to **100k** to cut down the area consumption.
3. Do the DC and AC analysis again to ensure that the open loop gain is still enough to meet the spec.

2. Second Stage

The second stage feedback loop is drawn by the red line. R3 and R4 sense the common mode of $\text{V}_{\text{out1,out2}}$, and create a negative feedback by

controlling the gate voltage of $M_{11,12}$.

The design flow is similar to the first stage feed back loop. To ensured that Vout is biased properly, the Vout common mode can be adjusted by modifying the aspect ratio of $M_{9\sim12}$.

3. Result

The feedback loop would set $V_{x,y}$ at $0.7V$ and $V_{out1,out2}$ at around $0.7V$. $R_1 = R_2 = 100k\Omega; R3 = R4 = 500k\Omega$. Due to the application of CMFB Loop, the circuit is much resistant to processing variations and easier to design.

(b) Verify the Specifications

1. Open Loop Gain

$$A_0 = 3715 = 71.4\text{dB}$$

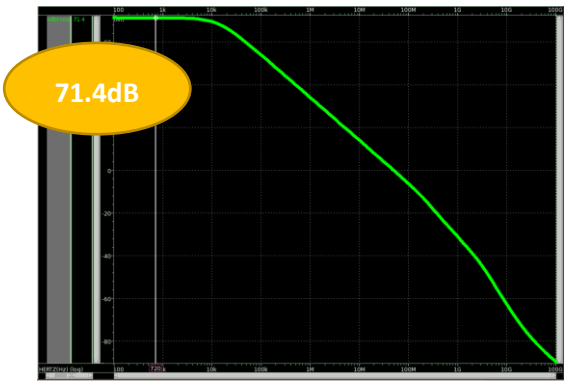


Fig. 6 Bode' Plot of Op-amp

2. Unity Gain Bandwidth/Phase Margin

$$\omega_t = 49.6\text{GHz}; \text{PM} = 80^0$$

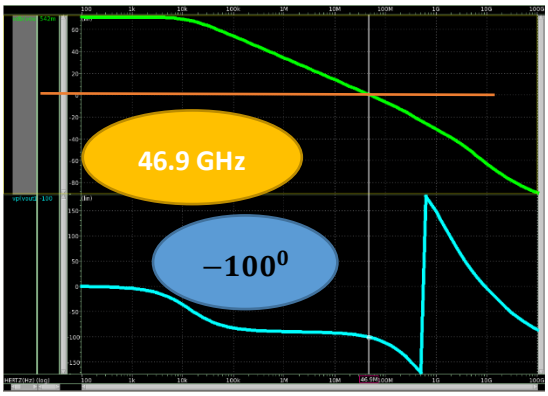


Fig. 7 ω_t/PM of Op-amp

3. Closed Loop

Using $10k\Omega/20k\Omega$ Resistor to produce 6.01dB closed loop gain

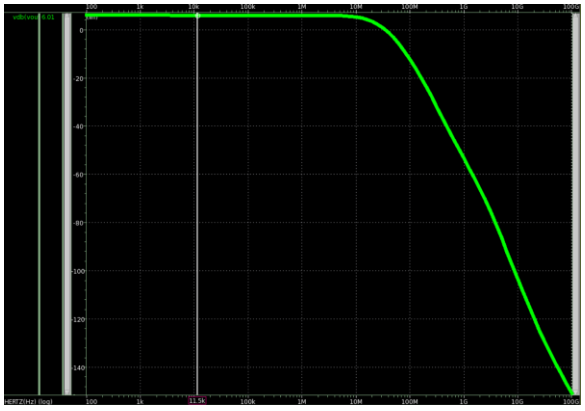


Fig. 8 Closed loop Bode' plot of Op-amp

4. Slew Rate

It takes 6.65ns to goes from -0.2V to 0V, so the slew rate is:

$$\frac{0.2\text{V}}{6.65\text{ns}} = 30V/us$$

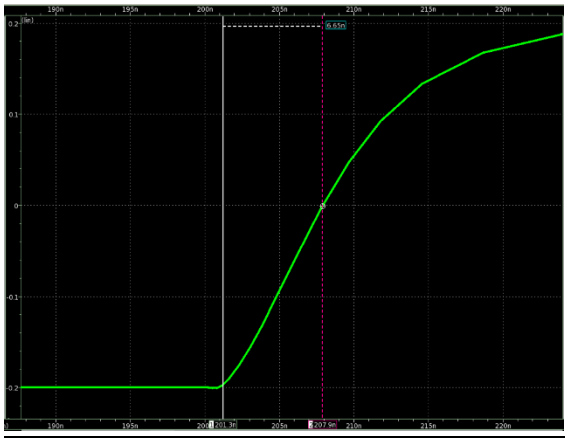


Fig. 9 Step Response of closed loop Op-amp

5. Power

The total power dissipation is 1.932mW

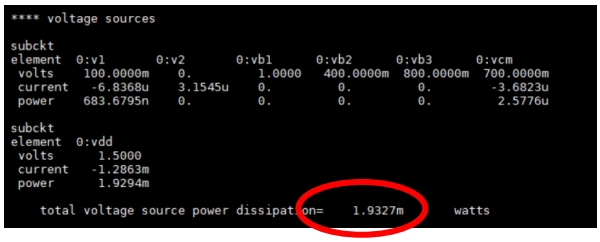


Fig. 10 Power Consumption of Op amp in .lis file

6. Output Differential Swing

Measured at closed loop gain =2 . The green line is (vout1-vout2) and red line is (vs1-vs2). The linear range of (vout1-vout2) goes from -1.3V to 1.3V, which means that **output differential swing is 2.6V**

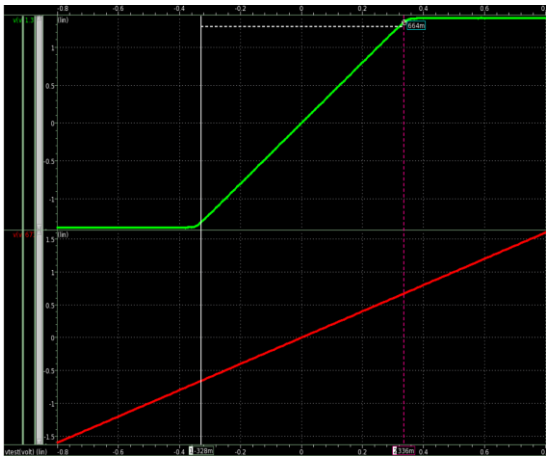


Fig. 11 Output Swing of Op-amp

(C) Settling Time/PSRR

1. Settling Time

Sending $\pm 0.1V_{ac}$ to input, the output swing should be $\pm 0.2V$. To observe the settling time with error less than 1%, the time between $-2V$ and $0.198V$, which is **33.7ns.**

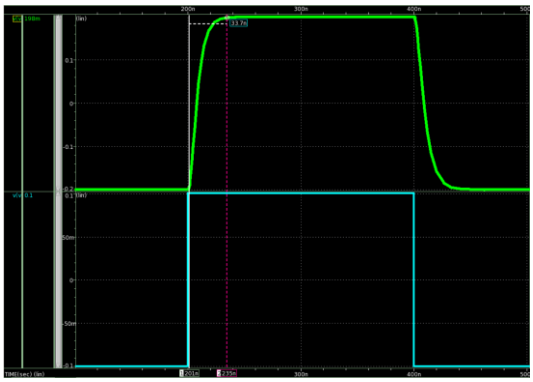


Fig. 12 Step response of closed loop Op-amp

2. PSRR

The mid band PSRR is around -212dB, and PSRR reach -270dB at high frequency. This measurement exhibits that OP-amp is very resistant to Power supply noise.

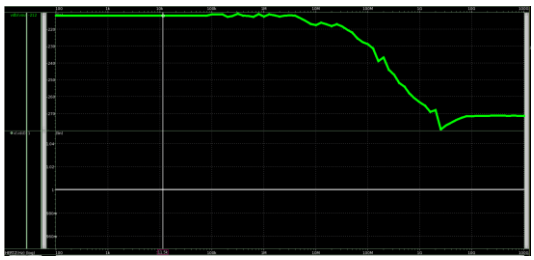
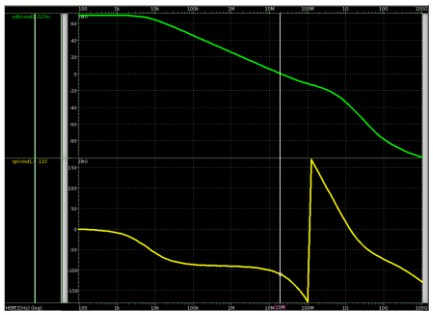


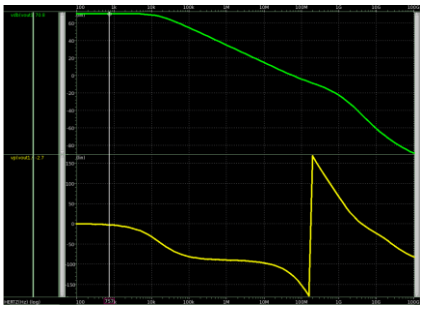
Fig. 13 PSRR of Op-amp

(D) Extra Test: PVT Test

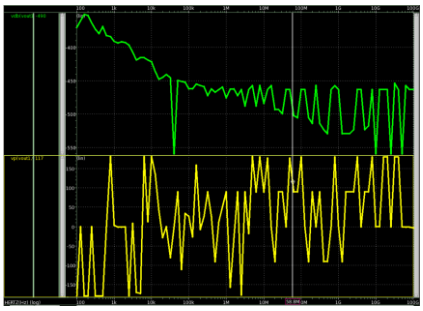
SS: gain = 69.8dB, PM = 70^0



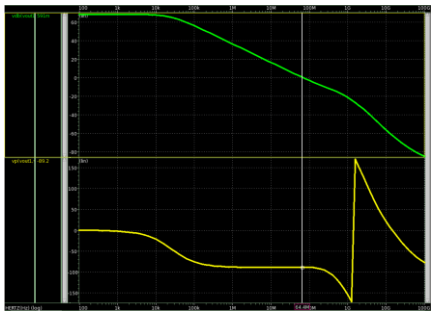
FS: gain =70.8dB, PM= 50^0



SF break



FF: gain=68.6dB phase=90^0



The circuit can sustain most of process variations, and with still acceptable PM. However, when it goes to SF region, the circuit tends to break.