LNA for Ultra-Wideband Wearable Device

Shih-Ming Huang, Wei-Chang Hou, Lin-Yung Kun, Hou-En Chen, and De-Lun Fan

***Abstract*—A low-power 0.18- μm CMOS low-noise amplifier for Ultra-Wideband applications is presented. The power reduction is achieved by the current-reused structure. Along with forward body bias technique, the circuit possess a significant voltage down scaling, which can further decrease the total power consumption. By using the shunt resistive feedback in the input and output stage, the broadband impedance matching can be obtained. The LNA exhibits a 11.5 dB gain with only 1 dB fluctuation over the entire UWB bandwidth from 3.1 to 10.6 GHz, and a minimum noise figure of 3 dB. The power dissipation is only 3.6 mW, with small chip area (0.7 mm2), which is a suitable solution for low-power applications**

I. Introduction

Over the last decades, advancements in radio communication technology have changed our life. Due to the growing demand of high data-rate wireless communications, the standard of Ultra-Wideband (UWB) was set up by the Federal Communications Commission (FCC) in 2002. The spectrum ranges from 3.1 to 10.6 GHz, with 7.5 GHz bandwidth. UWB is a radio technology that can use a very low energy level for short range, high data-rate communications, and can co-exist with the licensed spectrum. It is known as pulse radio, which transmits information by generating radio energy at specific time intervals. Because the pulse signals occupy a large bandwidth, it can achieve high data-rate wireless communications (up to 480 Mb/s). In addition, it provides a low power level (limit to −41.3 dBm/MHz) transmission, which is suitable for wearable device applications.

As the first stage of an UWB receiver, the low-noise amplifier (LNA) with a wide-band operation is critical to the overall receiver performance. It is required to amplify the very low power signal comes from an antenna and decreases the noise as much as possible. Several challenges in the design of LNA are encountered, such as the wide-band input matching, low noise figure to enhance receiver sensitivity, flat and high gain to suppress the noise of the overall system, low power consumption to increase battery life, and small die area to reduce the cost.

Many topologies have been presented in wide-band LNA designs, such as balanced amplifiers, distributed amplifiers, common gate amplifiers, current-reused amplifiers, and resistive shunt feedback. The balanced amplifier and distributed amplifier can provide wide-band characteristics, good linearity and sufficient input/output matching conditions. But the topologies need much more transistors, which occupy a significant chip area and consume more power. Using common gate amplifier at the 1st stage can result in good impedance matching due to the constant wide-band input impedance of $1/g_m$. However, the common-gate stage suffers from poor noise performance. In this paper, we adopt the current-reused structure for low power consumption. In addition, we introduce forward body bias technique to further lower the circuit voltage level. Last but not least, a shunt resistive feedback in the first and second stage is employed to get broadband input matching. The circuit is designed in a 0.18- μm CMOS technology for low cost demand in wearable device applications.

II. Paper Survey

We first found the papers for ultra-wide band which operating band is 3.1GHz ~10.6GHz in nearly ten years as shown in Table I. For wearable device, the main characteristic we focus on is the power consumption of the individual circuits. Compare to those papers, we pick three papers as our reference papers which the power is lower than 10 mW. All three papers used current-reused method to lower power dissipation. In [4] and [10], additional foward body bias technology is used for further power reduction. In this paper, we will combine the technologies stated above and additional output matching network to reach better performance on power and flat gain over the operating frequency band than those papers under 0.18μm CMOS process.

III. UWB LNA Circuit Design And Analysis

A. UWB LNA Circuit Topology

Fig. 1 illustrates the circuit schematics of the proposed wearable ultra-wideband LNA. The technique of this two-stage cacade circuit included current reused structure, forward body bias, source degeneration and RLC feedback to approach wideband input matching and low power characteristic for wearable used. The design goals of this work are shown in Table II.

TABLE I
THE COMPARISON TABLE OF THE REFERENCE PAPERS

Ref.	BW (GHz)	S_{21} (dB)	S_{11} (dB)	S_{12} (dB)	NF (dB)	Power Consumption (mW)	Area (mm^2)	Process	Year
[2] (LNA-1)	3.1-10.6	11.2 $\pm$ 2.3	-11.8~ -40.9	<-27.7	3.61-4.68	10.34	0.565	0.18 µm CMOS	2010
[2] (LNA-2)	3.1-10.6	12.26 $\pm$ 0.63	-8.6~ -21.3	<-26	3.74-4.74	10.34	0.536	0.18 µm CMOS	2010
[2] (LNA-3)	3.1-10.6	7.92 $\pm$ 0.23	-17.5~ -33.6	<-25.8	2.5-4.56	10.68	0.435	0.13 µm CMOS	2010
[6]	3.1-10.6	12.4	<-7.3	--	2.7-3.7	14.4	0.031	0.13 µm CMOS	2010
[7]	3.1-10.6	7-12	<-13.5	<-43	5.27-7	4.5	1.03	0.18 µm CMOS	2010
[10]	2.6-10.2	12.5	-9	<-45	3-7	7.2	0.64	90 nm CMOS	2011
[9]	3.1-10.6	10.2 $\pm$ 0.9	<-8.8	--	3.2-4.7	16	--	0.18 µm CMOS	2013
[8] Chip 1	3.1-10.6	9.7	<-10	<-26	4.2	11	0.926	0.18 µm CMOS	2013
[8] Chip 2	3.1-10.6	13.2	<-10.3	<-41.6	3.33	9.3	0.91	0.18 µm CMOS	2013
[1]	3.1-10.6	$\geq$ 20	<-10	--	1.2-2.6	12.6	--	90 nm CMOS	2014
[4]	3.1-10.6	11.58 $\pm$ 1.03	<-10.54	<-27.36	3.21-3.95	5.2	0.69	0.18 µm CMOS	2017
[3] (Fully integrated inductors)	3.1-10.5	11	-9~-37.5	--	1.8-2.6	45	1.5	0.15 µm pHEMT	2018
[3] (L_2/L_3 bondwire inductors)	3.7-10.5	12	-8~-25	--	1.4-2	45	1.5	0.15 µm pHEMT	2018

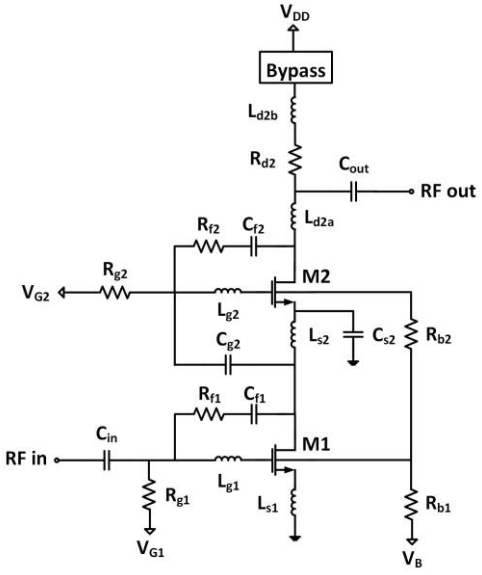


Fig. 1. Circuit architecture of this work.

TABLE II
THE DESIGN GOALS OF THE CIRCUIT ARCHITECTURE

Technology		0.18µm
Freq	(GHz)	3.1-10.6
NF	(dB)	5
Gain	(dB)	10
Power	(mW)	10
V_{DD}	(V)	1
Area	(mm^2)	0.8

B. M1 Transistor Parameters Selection

To decide the gate width (W) and the number of fingers (NR) of transistor M1. First, fix NR to 64, sweep W from 2µm to 8µm. As Fig. 2 shown, the minimum noise figure (NFmin) increase with W while the maximum gain (MaxGain) decrease. Thus, we first choose W as 3 µm. Next, under W = 3µm, sweep NR from 4 to 64. From Fig. 3, we observe that the NFmin increase while the MaxGain decrease with NR. Then considering under the same total width equal to 168µm, there are four sets of width and number of fingers: 1) 7µm × 24, 2) 6µm × 28, 3) 4µm × 42, 4) 3µm × 56. As

Fig. 4 shown, we finally choose 3μm × 56 for the better performance of NFmin and MaxGain.

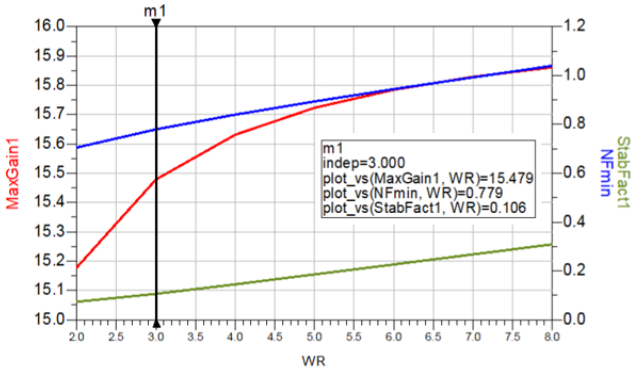


Fig. 2. Fix NR to 64, sweep W from 2-8 μm.

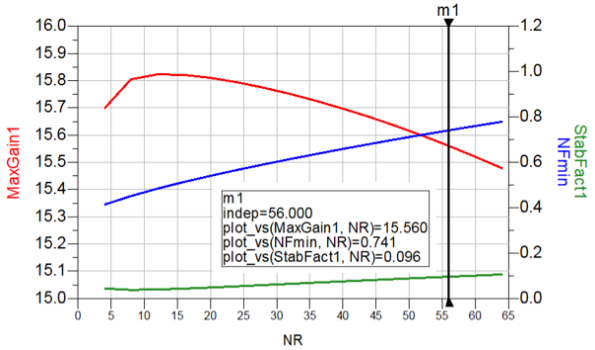


Fig. 3. Fix W to 3 μm, sweep NR from 4-64.

After deciding the width and the number of fingers, we need to decide the bias point of the M1 transistor. For low power LNA design, we choose the smaller drain current approximately at 50% of the peak of g_m which indicate as 3mA.

In order to lower the power consumption, using forward body bias technique to choose the appropriate V_{BS} and V_{GS}. In Fig. 5, we use ADS to simulate the drain voltage of transistor M1 under same drain current (3μm) and different V_{BS}. Cause there are two transistors cascade in the circuit design, the drain voltage of transistor M1 can't be too high. Under this consideration, we choose V_{BS} equal to 0.6 V and V_{GS} equal to 0.5V to lower the voltage level of the circuit.

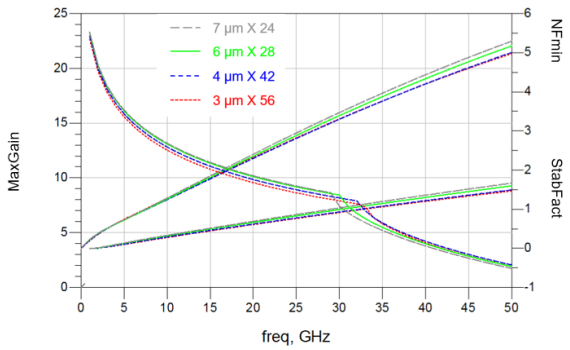


Fig. 4 Four sets under same total width equal to 168 μm

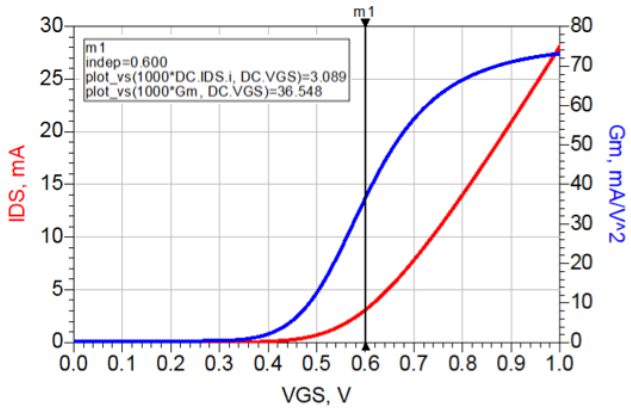


Fig. 5

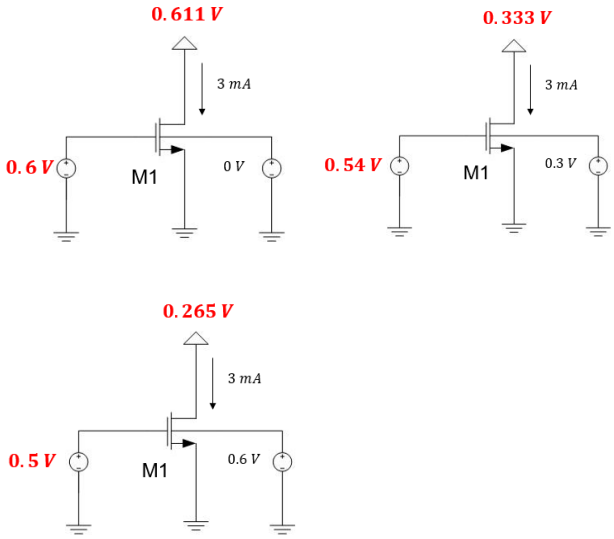


Fig. 6

For the consideration of M1 transistor, we use RC feedback at M1 to stablize the circuit (Fig. 7). As shown in Fig. 8, the stability factor increases with the increasing R_{f1}. Because we will add inductors at the following steps which the stability factor will increase. Thus, here we choose $R_{f1} = 550\Omega$ which the stability factor is close to 1.

After considering only M1 transistor, adding M2 transistor to check the stability factor (Fig. 9). From Fig. 10, the stability factor is much greater than 1 indicate that this two-stage cacade circuit currently.

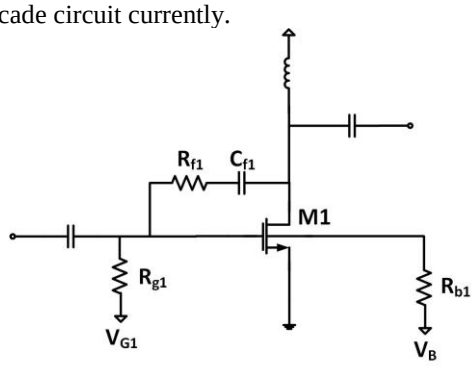


Fig. 7

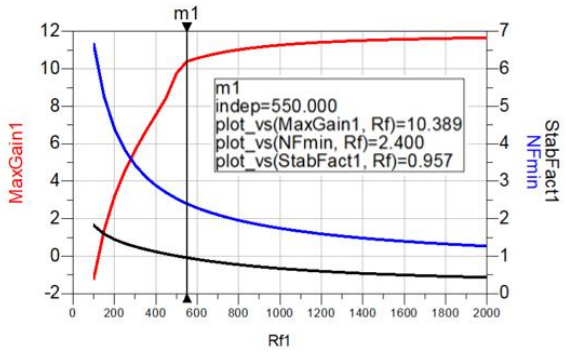


Fig. 8

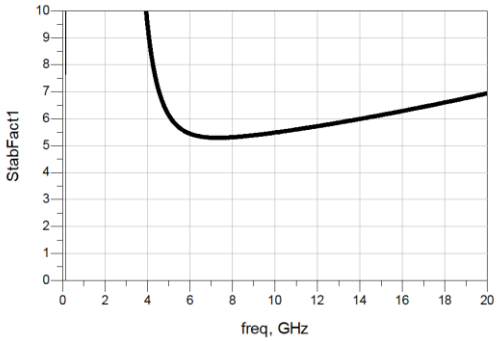


Fig. 9

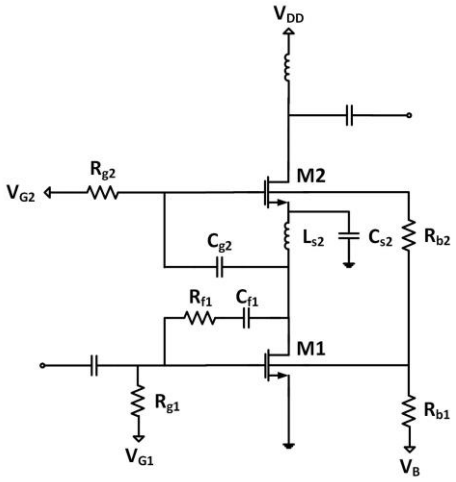


Fig. 10

C. *Wideband Input Matching Network Design*

Before design the wideband input matching network, we first extract the MOSFET parameters under the DC bias voltage decided in the previous section as shown in Fig. 11. Extracting by small signal model method, we get $C_{gs1} = 139fF$, $C_{gs2} = 83fF$, $g_{m1} = 39mS$, $g_{m2} = 32mS$.

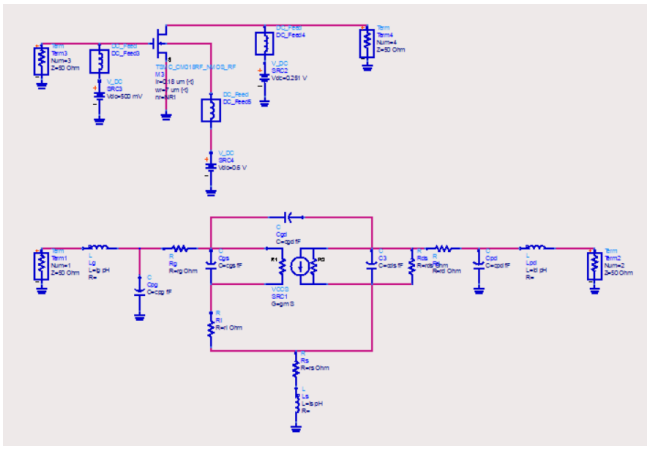


Fig. 11

1) Current Gain Consideration

To achieve gain boosting at higher frequency band, we first calculate the current gain of the second transistor from Eq. 1 which derived from the small circuit model of transistor M2 as shown in Fig.13. From Eq.2 we know that the maximum current gain appears at the second resonance point ω_{o2}. Follow the design rule of LNA, it is more difficult to reach high gain at higher frequency band. Thus, we let ω_{o2} operate at 10.6GHz the highest point over the frequency band to meet the requirement of high gain over the operating frequency band. For decided ω_{o2}, we can derive C_{g2}, L_{g2} and C_{in2} (as shown in Fig.12) from Eq.3.

$$\frac{i_{d2}}{i_{d1}} = -j\frac{g_{m2}}{\omega C_{gs2}\left(1+\left(\frac{1}{sL_{s2}}+Y_{sub}\right)sL_{g2}\left[1-\left(\frac{\omega}{\omega_{o2}}\right)^2\right]\right)} \quad (1)$$

$$\left|\frac{i_{d2}}{i_{d1}}\right|_{max} = \left|\frac{i_{d2}}{i_{d1}}\right|_{\omega=\omega_2} \quad (2)$$

$$\omega_{o2} = \frac{1}{\sqrt{L_{g2}C_{in2}}}, C_{in2} = \frac{1}{\frac{1}{C_{gs2}}+\frac{1}{C_{g2}}} \quad (3)$$

$$\omega_{o1,H} = \frac{1}{\sqrt{C_{gs1}(L_{s1}+L_{g1})}} \quad (4)$$

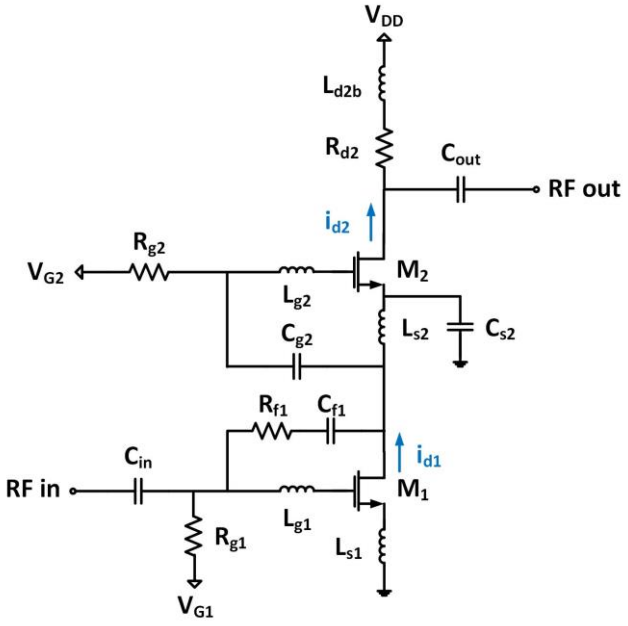


Fig. 12

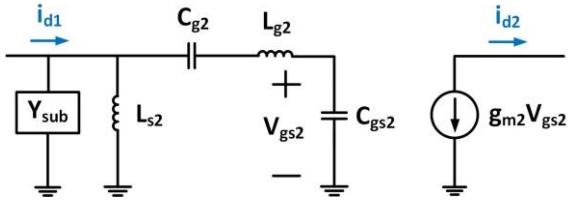


Fig. 13

2) S_{11} Consideration

By generating two notch point separately at higher and lower frequency band, we can achieve wide band input matching. From Eq. 5 and Eq.6, the higher resonance point ($\omega_{o1,H}$) is related to the parameter of transistor M1, L_{s1} and L_{g1}. From the parameters' extraction of MOSFET, we already know $C_{gs1} = 130\ fF$. For $\omega_{o1,H}$ operates at 10.6 GHz, $L_{s1} + L_{g1} = 1.6\ nH$. From Eq.6, the lower resonance point ($\omega_{o1,L}$) is related to the parameter of transistor M2, L_{s2} and L_{g2}. For $\omega_{o1,L}$ operates at 6 GHz, L_{s2} should choose at 6 nH.

$$\omega_{o1,H} = \frac{1}{\sqrt{C_{gs1}(L_{s1} + L_{g1})}} \tag{5}$$

$$\omega_{o1,L} = \frac{1}{\sqrt{C_{in2}(L_{s2} + L_{g2})}} \tag{6}$$

Table 2 list the parameters' initial design of the matching network and S_{11}, S_{21} and S_{22} are shown in Fig. 14 . From Fig. 15, we can see that S_{11} of the matching network is close to the center of noise figure and gain circles under 4GHz, 6.5GHz and 8.5GHz which indicate the current design can reach both low noise and high gain.

TABLE III
THE DESIGN GOALS OF THE CIRCUIT ARCHITECTURE

Parameters	Initial Design
$L_{g1} + L_{s1}$	1.6 nH
L_{s2}	6 nH
L_{g2}	3 nH
C_{g2}	0.6 pF
R_{fb}	550 Ω
C_{fb}	0.9 pF

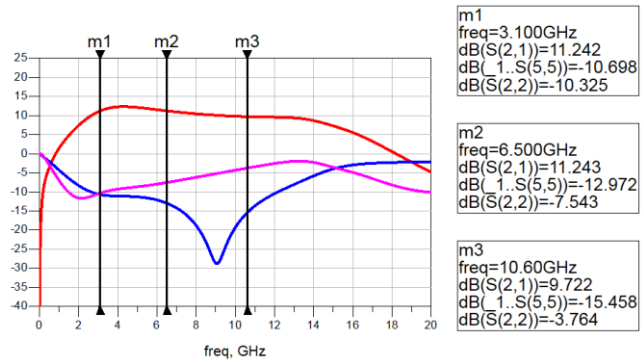


Fig. 14

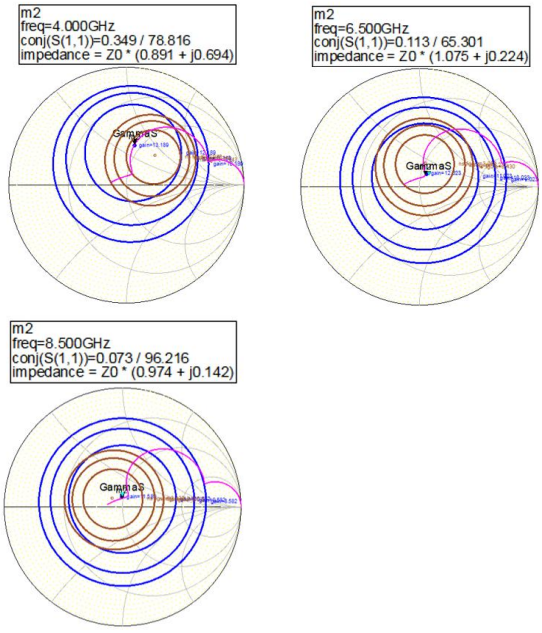


Fig. 15

D. Flat Gain and Output Matching

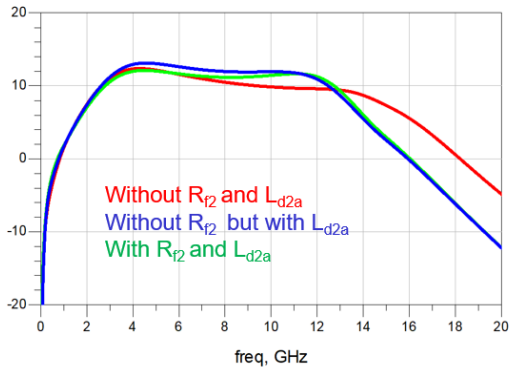


Fig. 16

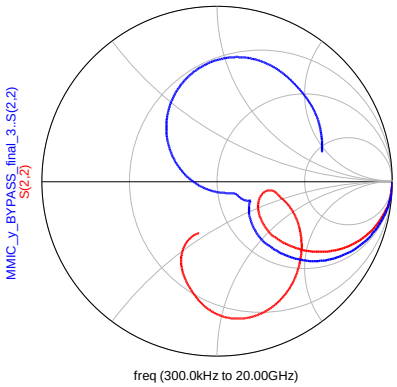


Fig. 17

E. Simulation Results

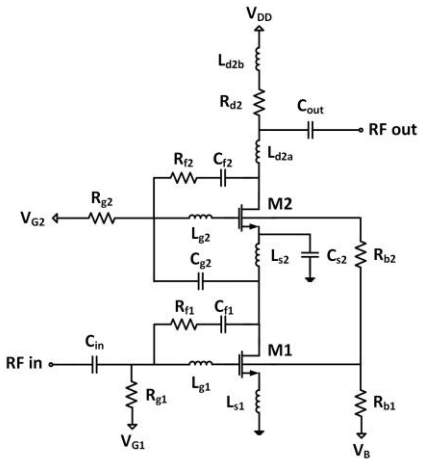


Fig. 18

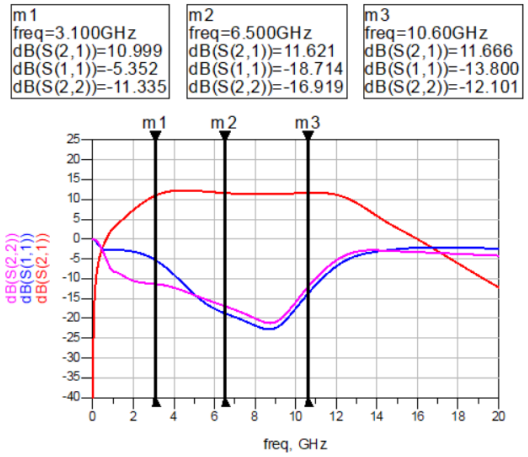


Fig. 19

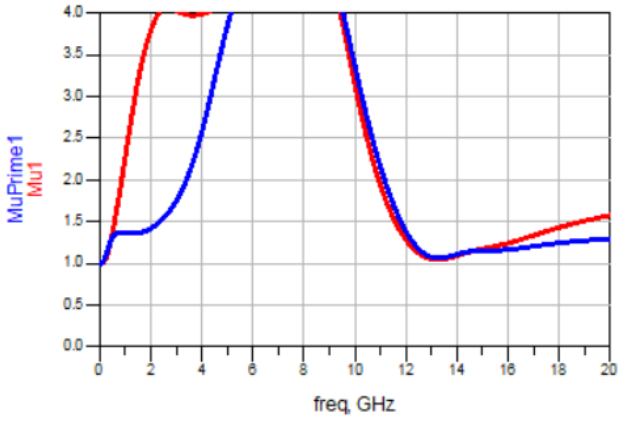


Fig. 20

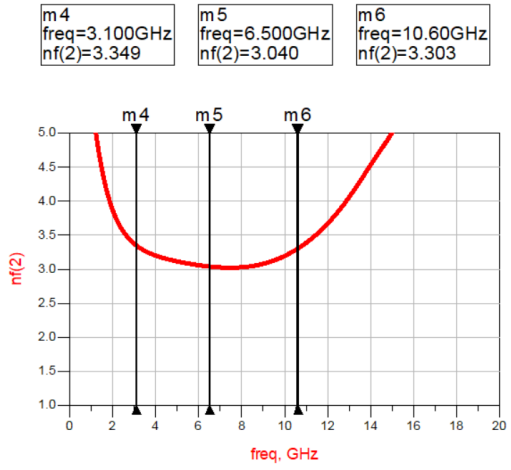


Fig. 21

F. Bypass Circuit Design

In order to minimize the area, the smaller capacitor is designed on-chip and the rest is designed off-chip. Two parts of the bypass circuitry are connected with the bondwire which is modeled as L_{wire}.

Series of 10pF Moscap and a resistor compose the on-chip

bypass circuitry which directly bypasses rf signals at the higher operating frequency band, the series resistor can de-Q the bypass circuit to eliminate unwanted resonances caused by the capacitor and the bondwire parasitic inductance. For off-chip bypass circuitry, two-stage of series inductance and capacitor with larger values bypass signals at lower frequencies.

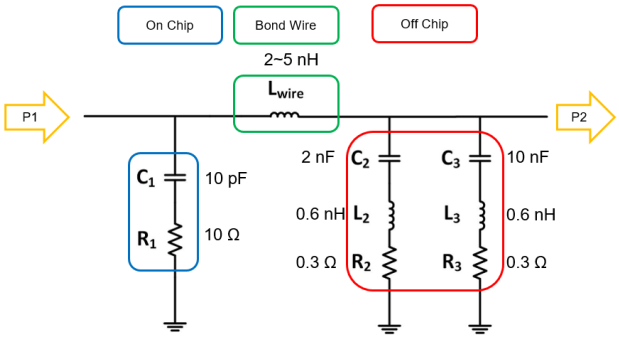


Fig. 22

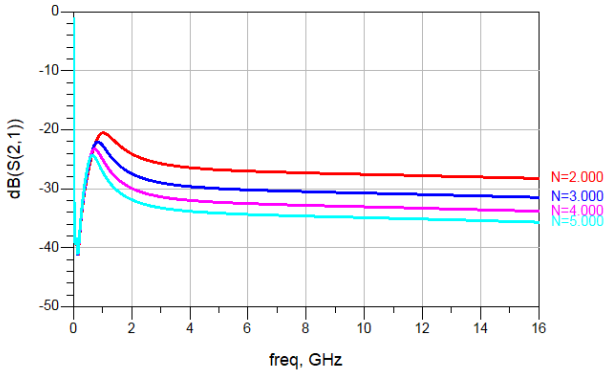
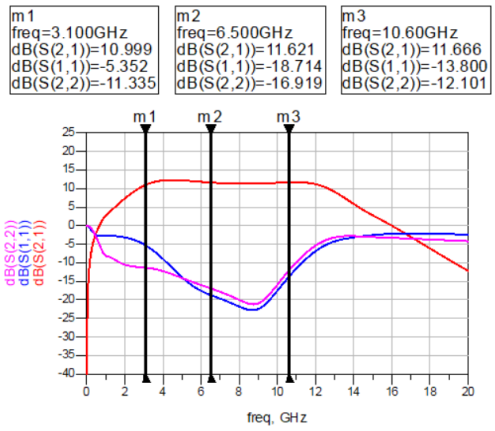
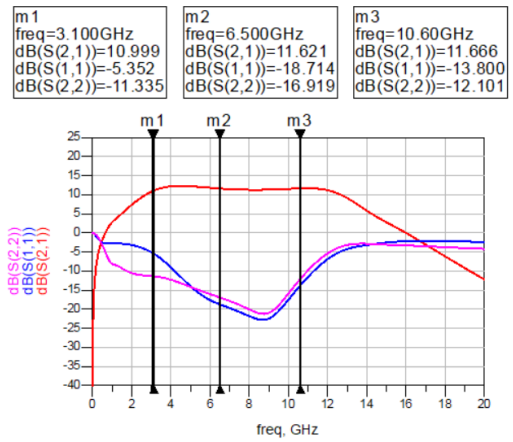
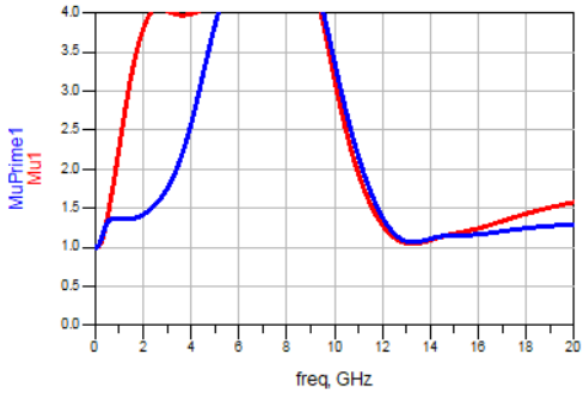


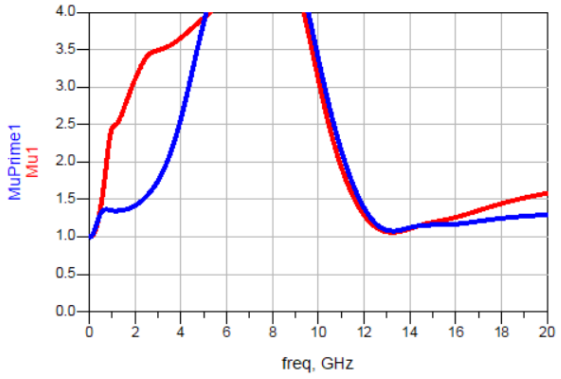
Fig. 23

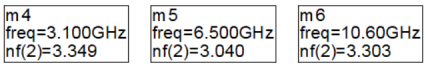
G. Complete Circuit with Bypass Circuit Design

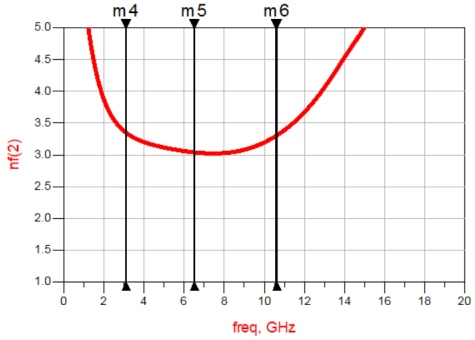












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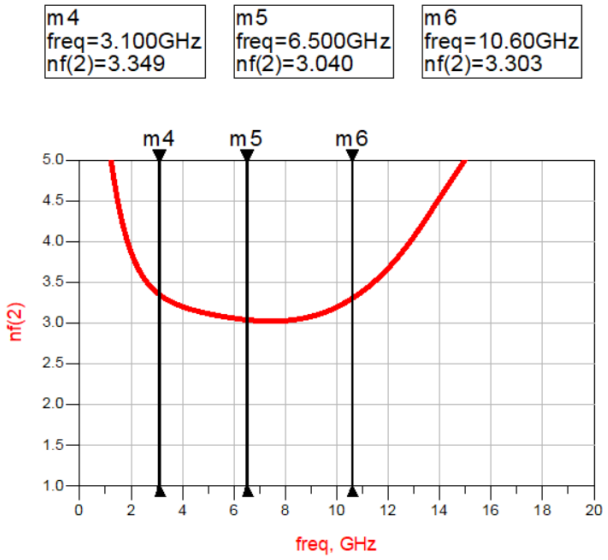
Goal	3.1-10.6	10	--	--	5	10	0.8	0.18 µm CMOS	2020
This Work	3.0-12.25	11.52 ± 1	<-5	<-24	3.0-3.8	3.59	0.56	0.18 µm CMOS	2020



IV. LAYOUT AND FULL-WAVE ANALYSIS

A. Overview

The layout of the proposed circuits is shown in Fig. 14. To comply with the RF probe station in NTU, we assign the RF input port on the left-hand side, RF output port on the right-hand side, and DC pads on the top and bottom side. The center-to-center spacing of the pads are 100 µm and the width is 50 µm. The arrangement of the pads ensures feasibilites of future measurement.

The parasitic effect of the inductors plays a crucial role in the performance of the circuits. To reduce the parasitic capacitance, the ground plane is kept out of the region under the inductors. The parasitic resistor could be reduced by arranging the inductors on the top layer. Furthermore, the mutual coupling of inductors could be improved by directing the current of all inductors in counter-clockwise direction. Because the magnetic fluxes of the same polarization repel each other, the inductors of the same direction of current flow have less mutual coupling effect.

Since the model of capacitors and resistors in 0.18-µm CMOS process is accurate enough for the UWB application, full-wave analysis will only be done on transmission lines and inductors. However, the number of meshes remain too big to be solved by a personal computer, and thus the circuit is divided into three sub-circuits, including matching network of M_1 and M_2 and the gain-boosting inductor, and simulated.

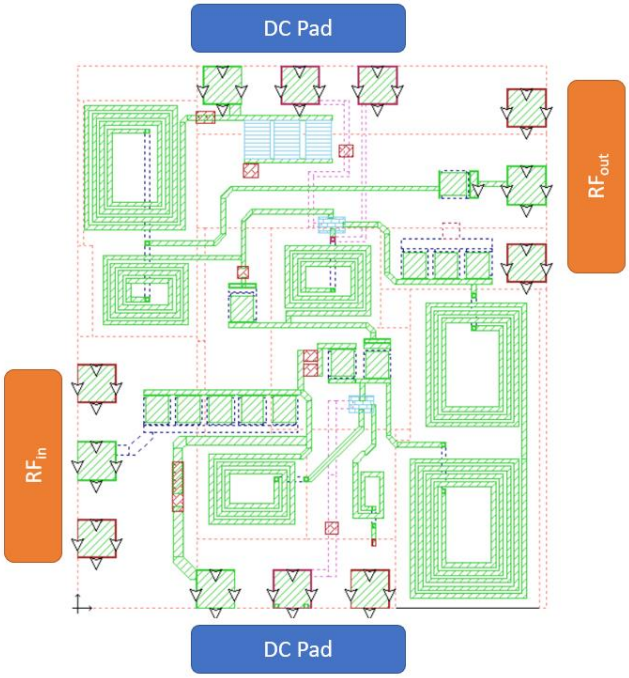


Fig. 24. The layout of the proposed circuit designed on Sonnet. The orange and blue boxes indicate the functions of the pads.

A. Matching network of M_1

The sub-circuit of the matching network of M_1 is shown in Fig. 15. The effective inductance calculated from S_{11}, shown in Fig. 16 and 17, is close to the designated design in the schematic.

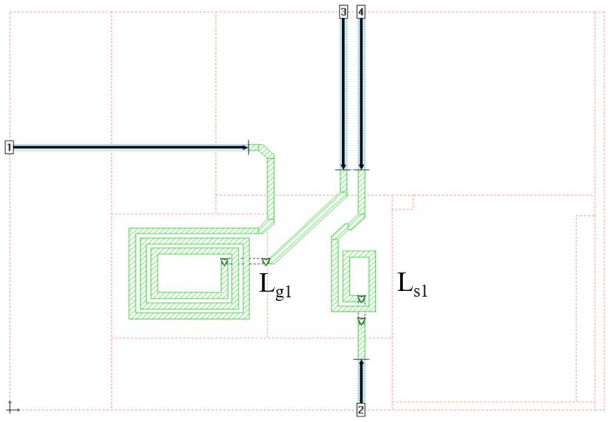


Fig. 25. The matching network of M_1 designed on Sonnet.

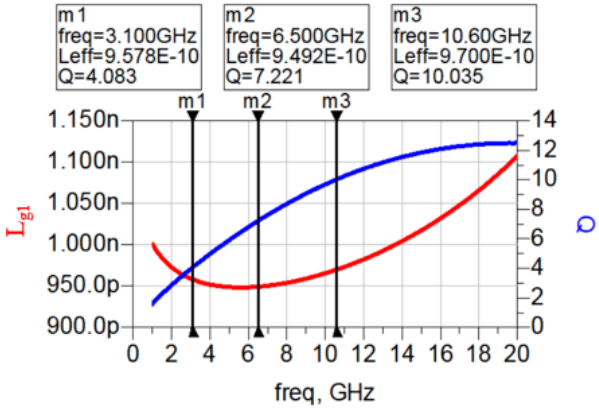


Fig. 26. Inductance and quality factor of L_{g1}. The designated value of L_{g1} is 1 nH.

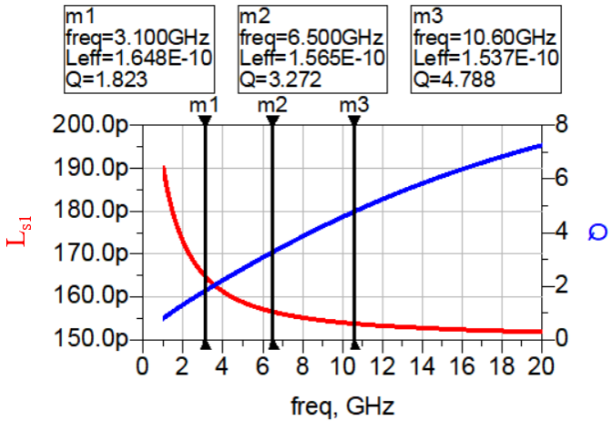


Fig. 27. Inductance and quality factor of L_{s1}. The designated value of L_{s1} is 200 pH

A. *Matching network of M_2*

The sub-circuit of the matching network of M_1 is shown in Fig. 18. The effective inductance is shown in Fig. 19 and 20. The inductance of L_{d2a}+L_{d2b} is close to designated value, but the inductance of L_{g2} is a little higher than the value of design.

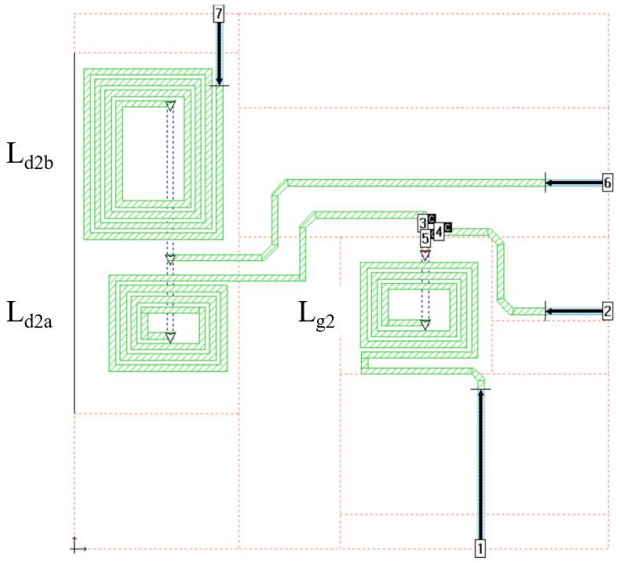


Fig. 28. The matching network of M_2 designed on Sonnet.

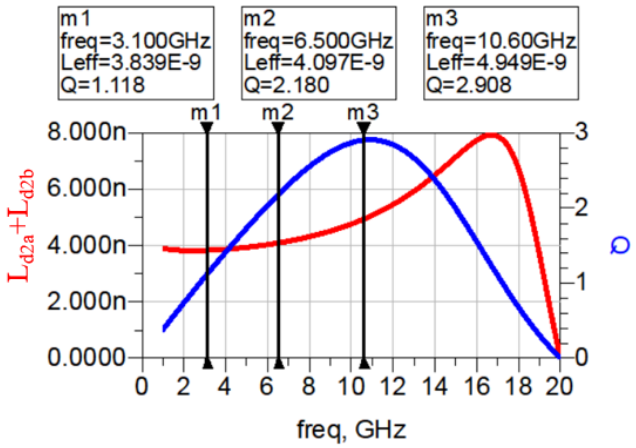


Fig. 29. Inductance and quality factor of L_{d2a}+Ld2b. The designated value of L_{d2a}+L_{d2b} is 4.6 nH.

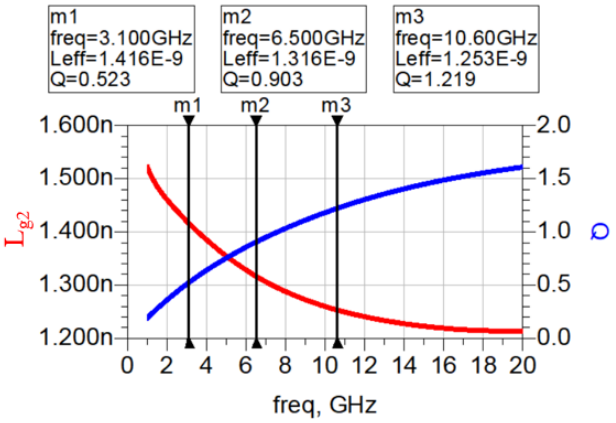


Fig. 30. Inductance and quality factor of L_{g2}. The designated value of L_{g2} is 1 nH.

B. *Gain Boosting Inductor*

The gain boosting inductor should be big enough to block the RF signal from the drain of M_1 to the source of M_2. To implement an inductor with high inductance and high resonance frequency, we connect two inductors in series.

The layout is shown in Fig. 21 and the effective inductance is shown in Fig. 22.

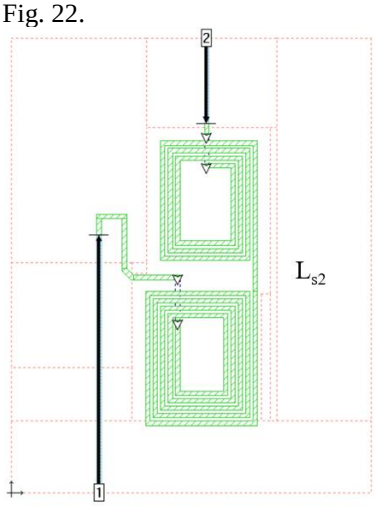


Fig. 31. The gain-boosting inductor designed on Sonnet.

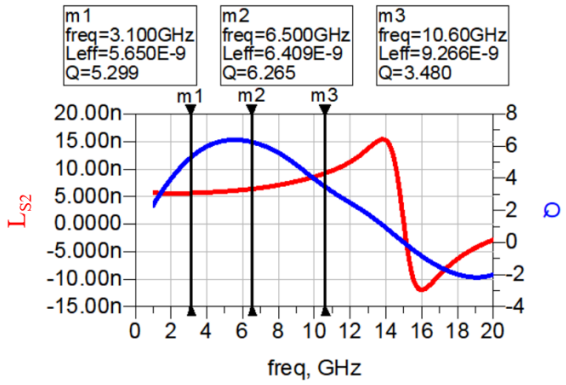


Fig. 32. Inductance and quality factor of L_{s2}. The designated value of L_{s2} is 6nH

V. Conclusion

This paper demonstrates a LNA addressed to 3.1 – 10.6 GHz UWB low-power application. The circuit is designed using current-reused topology, with forward body bias technique to further decrease the power dissipation. It is shown that the designed LNA achieves flat gain, low noise, low-power consumption, and small chip area. It provides a suitable solution for low power UWB LNA and designed using low cost 0.18- μm CMOS technology.

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